Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. The following listing provides the amended claims with the amendments marked with deleted material crossed out and new material underlined to show the changes made.

Listing of Claims:

1. (Currently Amended) For a layout that has multiple layers, a method of generating a multi-layer topological path comprising:

a) specifying a set of path expansions from a first topological item to a second topological item, wherein the second topological item is on a first layer of the layout; and

b) for a potential via expansion from the second topological item to a third topological item on a second layer of the layout,

identifying a first region on the first layer for the second topological item;

identifying a second region on the second layer for the third topological item;

determining whether an intersection of the first and second regions is ~~sufficiently large to contain a via~~ larger than a threshold area; and

if the intersection is ~~sufficiently~~ larger than the threshold area, adding the potential via expansion to the specified set of path expansions.

2. (Currently Amended) The method of claim 1, wherein if the intersection is not ~~sufficiently~~ larger than the threshold area, discarding the potential via expansion.

3. (Original) The method of claim 1 further comprising:

before specifying the set of path expansions, decomposing the layout into a plurality of faces, wherein each face has a set of edges and an interior space between the edges;

wherein at least one of the second and third topological items represents an interior space of a face.

4. (Currently Amended) The method of claim 3~~claim3~~, wherein the second topological item represents an interior space of a first face on the ~~a~~ first layer, and the third topological item represents an interior space of a second face on the second layer.

5. (Original) The method of claim 3, wherein the layout is an IC layout.

6. (Currently Amended) The method of claim 5, wherein the IC layout includes a plurality of routable elements, wherein decomposing the layout comprises:

specifying a plurality of nodes along boundaries of the routable elements; and

defining edges between the nodes.

7. (Original) The method of claim 1, wherein each path expansion starts at a source topological item and ends with a destination topological item.

8. (Currently Amended) A computer program stored on a computer readable medium, wherein the computer program generates, for a layout that has multiple layers, a multi-layer topological path, the computer program comprising:

a) a first set of instructions for specifying a set of path expansions from a first topological item to a second topological item, wherein the second topological item is on a first layer of the layout;

b) for a potential via expansion from the second topological item to a third topological item on a second layer of the layout,

a second set of instructions for identifying a first region on the first layer for the second topological item;

a third set of instructions for identifying a second region on the second layer for the third topological item;

a fourth set of instructions for determining whether an intersection of the first and second regions is ~~sufficiently large to contain a via~~ larger than a threshold area; and

a fifth set of instructions for adding the potential via expansion to the specified set of path expansions, when the intersection is ~~sufficiently~~ larger than the threshold area.

9. (Original) The computer program of claim 8 further comprising a sixth set of instructions for identifying another potential expansion from the second topological item when the intersection is not larger than the threshold area~~when when the intersection is not sufficiently large~~.

10. (Original) The computer program of claim 8 further comprising:

a sixth set of instruction for decomposing, before specifying the set of path expansions, the layout into a plurality of faces, wherein each face has a set of edges and an interior space between the edges;

wherein at least one of the second and third topological items represents an interior space of a face.

11. (Currently Amended) The computer program of claim 10, wherein the second topological item represents an interior space of a first face on the ~~a~~ first layer, and the third topological item represents an interior space of a second face on the second layer.

12. (Original) The computer program of claim 10, wherein the layout is an IC layout.

13. (Currently Amended) The computer program of claim 12, wherein the IC layout includes a plurality of routable elements, wherein the sixth set of instructions comprises:

a seventh set of instructions for specifying a plurality of nodes along boundaries of the routable elements; and

an eight set of instructions for defining edges between the nodes.

14. (Original) The computer program of claim 13, wherein each path expansion starts at a source topological item and ends with a destination topological item.

15. (New) For an integrated circuit layout that has multiple layers, a method of generating a multi-layer topological path comprising:

a) identifying a set of path expansions from a first topological item to a second topological item on a first layer of the layout;

b) identifying a first region on the first layer for the second topological item, and a second region on the second layer for a third topological item that is reachable from the second topological item through a via expansion;

c) determining whether an intersection of the first and second regions is larger than a threshold area; and

d) adding the potential via expansion to the specified set of path expansions when the intersection is larger than the threshold area.

16. (New) The method of claim 15 further comprising discarding the potential via expansion when the intersection is not larger than the threshold area.

17. (New) The method of claim 15 further comprising:

before specifying the set of path expansions, decomposing the layout into a plurality of faces, wherein each face has a set of edges and an interior space between the edges;

wherein at least one of the second and third topological items represents an interior space of a face.

18. (New) The method of claim 17, wherein the second topological item represents an interior space of a first face on the first layer, and the third topological item represents an interior space of a second face on the second layer.

19. (New) The method of claim 17, wherein the IC layout includes a plurality of routable elements, wherein decomposing the layout comprises:

specifying a plurality of nodes along boundaries of the routable elements; and

defining edges between the nodes.

20. (New) A computer program stored on a computer readable medium, wherein the computer program generates, for an integrated circuit layout that has multiple layers, a multi-layer topological path, the computer program comprising sets of instructions for:

a) identifying a set of path expansions from a first topological item to a second topological item on a first layer of the layout;

b) identifying a first region on the first layer for the second topological item, and a second region on the second layer for a third topological item that is reachable from the second topological item through a via expansion;

c) determining whether an intersection of the first and second regions is larger than a threshold area; and

d) adding the potential via expansion to the specified set of path expansions when the intersection is larger than the threshold area.

21. (New) The computer program of claim 20 further comprising a set of instructions for discarding the potential via expansion when the intersection is not larger than the threshold area.

22. (New) The computer program of claim 20 further comprising a set of instructions for decomposing the layout into a plurality of faces, before specifying the set of path expansions, wherein each face has a set of edges and an interior space between the edges; wherein at least one of the second and third topological items represents an interior space of a face.

23. (New) The computer program of claim 22, wherein the second topological item represents an interior space of a first face on the first layer, and the third topological item represents an interior space of a second face on the second layer.

24. (New) The computer program of claim 22, wherein the IC layout includes a plurality of routable elements, wherein the set of instructions for decomposing the layout comprises a set of instructions for:

specifying a plurality of nodes along boundaries of the routable elements; and

defining edges between the nodes.

Amendments to the Drawings

Attached to this Amendment are fifty-nine (59) sheets of formal drawings that include all of the Figures 1-83. Also attached are five (5) redlined sheets of drawings that include Figures 28B, 29B, 31B, 53A, and 53B. The redlined sheets show in red ink the additions that were made to the original Figures 28B, 29B, 31B, 53A, and 53B when these figures where formalized. The changes to Figures 28B, 29B, 31B, and 53B identify the source of the incoming arrows into the flowcharts illustrated in these figures, while the change to Figure 53A corrects the legend in this figure per the draftsperson's objection.